(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 356 020 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **89307640.6**

(51) Int. Cl.⁴: **G05F 3/24**

(22) Date of filing: **27.07.89**

(30) Priority: **15.08.88 US 232399**

(43) Date of publication of application:
28.02.90 Bulletin 90/09

(84) Designated Contracting States:
DE FR GB

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(54) A bias voltage generator for static CMOS circuits.

(57) A bias voltage generator for providing a voltage to bias static CMOS circuits, comprises a first compensation circuit arrangement (14) coupled to a power supply (+VDD) and a control node, the arrangement serving to generate at the control node a control voltage signal which compensates for tolerances in the power supply and device process parameters. A second compensation circuit arrangement (16) is coupled to the control node and serves to adjust the control voltage signal at the control node to compensate for device threshold voltage variations. The control voltage signal is inverted by an inverter circuit (18) to produce the output voltage of the generator.

The bias voltage generator is incorporated with the static CMOS circuits on a very large scale integration chip.

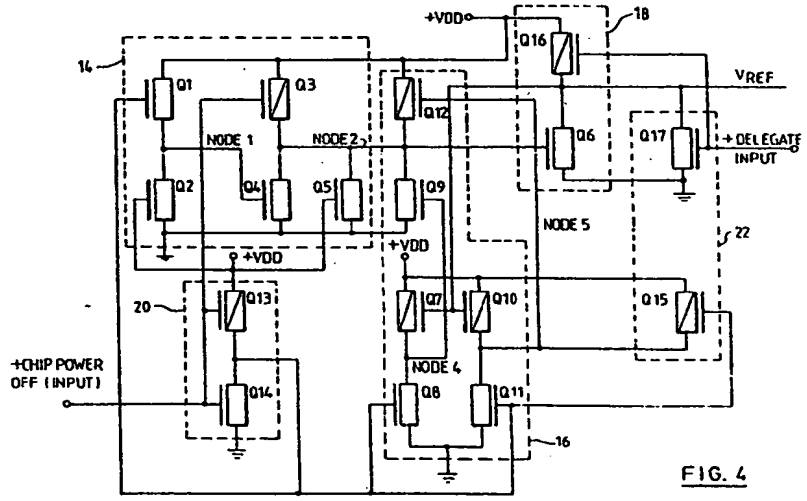

FIG. 4

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A BIAS VOLTAGE GENERATOR FOR STATIC CMOS CIRCUITS

This invention relates to a bias voltage generator for static CMOS circuits on a Very Large Scale Integration (VLSI) chip.

Most VLSI chips are now being designed with CMOS technology. It is believed that this trend is an attempt to capitalise on the improved power and performance characteristics which the CMOS technology provides. A typical VLSI chip is made up of thousands of circuit arrangements integrated on a single substrate. Some of these circuits, such as programmable logic arrays (PLA) and busses with several dotted drivers, require static power dissipating circuits in order to ensure proper operation.

One of the disadvantages of these static circuits is that, at worst case, they dissipate a relatively large amount of power. Because CMOS technology is a lower power technology, the presence of static circuits on the CMOS chip negates or undermines one of the benefits associated with the CMOS technology. Even though there are a plurality of different types of static CMOS circuits, an inverter circuit will be used to illustrate the relatively large amount of power which a typical static CMOS circuit dissipates.

Fig. 1 of the accompanying drawings is a schematic circuit of two typical inverter circuits which include a pair of P-channel devices Q26, Q30, and a pair of N-channel devices Q28, Q32. The source electrodes of the P-channel devices are connected to power supply (Vps) and the source electrodes of the N-channel devices are connected to ground potential. As is the usual practice with static CMOS circuits without availability of depletion NMOS devices, a P-channel FET device (Q26) is used as the load device. To provide the loading function, the gate electrode of Q26 is connected to the ground potential.

Current in the P-channel device can be expressed by the following simplified equation.

$I = K (Vgate - Vs - Vt)^2$, where

K is a function of parameters such as device width, length, gate oxide thickness, etc.

Vgate is the gate voltage of the P-channel device

Vs is the source voltage of the device, the power supply Vps

Vt is the threshold voltage of the device, typically -1 volt

For the P-channel device shown (Vgate - Vs) = Vps

Vps is the power supply voltage typically 5 ± 10%

Variations in the process parameters cause K to vary by as much as +/-60% between its -3 sigma limit and its +3 sigma limit. Varying the power supply voltage Vps from 4.5 volts to 5.5 volts increases the current in the P-channel device by 50%. Combining process variations and power supply tolerance, the current in the device can vary more than 400% from worst case (-3 sigma limit) to best case (+3 sigma limit) The -3 sigma and +3 sigma limits are statistical terms used to describe standard deviation from a nominal value.

Circuit performance can improve by a factor of 4 between worst case conditions and best case conditions. The designer usually has a worst case performance target for the circuit being designed. The designer then must be able to accommodate the power dissipation of the circuit at best case conditions. If there is a significant number of static circuits on a VLSI chip, the power dissipation at best case conditions will raise the chip's junction temperature, reduce its reliability and decrease the performance of other circuits.

A straightforward approach for solving the power dissipation problem is to package the chip in a ceramic casing. Such a casing usually has lower thermal resistance which keeps the junction temperature lower. Ceramic packages have lower thermal resistance than plastic packages but are more expensive and will make the component less competitive in the market place. In addition, the increased current stresses the current density limits of metal and contact structures further compounding the reliability issues.

The invention seeks to provide an on-chip circuit arrangement which biases static CMOS circuits to reduce the maximum power which is dissipated by the circuits while optimizing performance.

The invention provides a bias voltage generator for static circuits on a CMOS chip comprising a first compensation circuit arrangement coupled to a power supply and a control node, the arrangement serving to generate at the control node a control voltage signal which compensates for tolerances in the power supply and device process parameters; and a second compensation circuit arrangement coupled to the control node and serving to adjust the control voltage signal at the control node to compensate for device threshold voltage variations.

How the invention can be carried out will now be described by way of example, with reference to Figs. 2 to 5 of the accompanying drawings, in which:-

Fig. 2 shows variations in circuit delay and P-channel current versus process parameters and power supply tolerances;

Fig. 3 shows a VLSI chip including a bias voltage generator embodying the present invention;

Fig. 4 shows a circuit schematic of an on-chip bias voltage generator embodying the present invention; and

Fig. 5 shows a graph of the output voltage of the bias voltage generator as the current in the load device varies between -3 sigma and +3 sigma.

Fig. 2 shows a graph of P-channel load current and circuit delay for load device Q26 connected with its gate electrode connected to ground, as shown in the known inverter circuit arrangement of Fig. 1. The graph is helpful in understanding the power/performance problems which can be overcome by application of the present invention. As is shown in Fig. 2, the statistical distribution or spread from worst case (-3 sigma limit) to best case (+3 sigma limit) is plotted on the horizontal axis while the normalised circuit delay or P-channel current ratio is plotted on the vertical axis. The variation is caused by tolerances in the power supply voltage (Vps) and variation due to process and/or device parameters. The curve which represents P-channel current has a positive slope while the curve which represents circuit delay has a negative slope. A casual review of the graph shows that as the device performance varies between -3 sigma and +3 sigma the circuit performance varies by a ratio of 4.

The invention is concerned with a bias voltage generator to generate a bias voltage for application to the gate or control electrode of the load device Q26 (Fig. 1) The bias voltage generator compensates for variation due to process parameters and power supply tolerances which reduces the current variation in the load device from 400% to 40%.

Fig. 3 shows a VLSI chip 10 incorporating the present invention. The chip is exploded or magnified beyond its normal size for purposes of explanation. In actuality, the surface area of the chip is within millimeter range. Still referring to Fig. 3, the chip comprises a substrate 12 upon which a plurality of circuit arrangements are integrated. For brevity, only those circuit arrangements which are germane to explaining the present invention are shown, it being understood that the chip is populated with other circuit arrangements which are not shown in the sketch of Fig. 3. A plurality of static CMOS circuit arrangements 14-1 through 14-N are integrated on substrate 12. The static CMOS circuits may include PLAs, dotted circuits connected as bus structures, inverter circuits, etc. Each of these circuit arrangements includes a pull-up device which is biased by a bias voltage generator embodying the invention in order to minimize power dissipation in those circuit arrangements.

Thus, the present invention provides an on-chip bias generator which outputs a voltage Vreference (Vref) which is connected to the pullup devices (not shown) of each of the static CMOS circuits. For example, if each of the static CMOS circuits 14-1 through 14-N includes an inverter circuit such as the prior art inverter circuit of Fig. 1, the output Vreference from bias generator is connected to the gate electrode of the P-channel enhancement mode device Q1. With this configuration the power performance spread of the P-channel device is brought within acceptable range. Of course, a bias voltage generator embodying the present invention may be used to bias other types of static CMOS circuits.

Fig. 4 shows a circuit diagram of the voltage bias generator including a plurality of compensating circuits which are coupled through an output circuit to provide an output voltage which is applied to the gate electrodes of P-channel load devices. The bias voltage compensates for variations due to the process parameters of device channel length, channel width, and threshold voltage. The voltage is also adjusted for variation in the power supply voltage (VDD).

Generally, compensation is achieved by the technique of ratioing nominal parameters of two FET devices which are connected in series. A plurality of the series connected devices are arranged in parallel to provide a nominal value for a desired output voltage. The bias voltage generator includes a first compensation circuit arrangement 14, and a second compensation circuit arrangement 16. The first compensation circuit arrangement 14 compensates for tolerance in the power supply (VDD) and variation in the device parameters due to process variation. The second compensation circuit arrangement 16 adjusts for variation in device threshold voltage (Vt). The first and second compensation circuit arrangements 14 and 16 are connected to node 2. Node 2 in turn is connected by an output circuit arrangement 18 which produces V reference.

In the preferred embodiment of this invention, the output circuit arrangement 18 is an inverter circuit formed by devices Q6 and Q16. It should be noted that devices with a diagonal such as Q16 and similar ones are P-channel enhancement mode devices while devices with no diagonals such as Q6 and similar ones are N-channel enhancement mode devices. Circuit arrangements 20 and 22 provide testability to the voltage generator.

Still referring to Fig. 4, the first compensation circuit means 14 includes N-channel FET devices Q1 and Q2 which are connected in series between VDD and ground potential and a P-channel FET device Q3 which is also connected to VDD. The first compensation circuit 14 further includes a pair of N-channel FET

devices Q4 and Q5 which are positioned in parallel and connected to the drain electrode of Q3. The combination of Q3, Q4 and Q5 interconnects VDD to ground potential. Node 1 which is positioned between devices Q1 and Q2 is connected to the gate electrode of Q4. In operation, devices Q1-Q5 bias node 2 such that a desired bias voltage is achieved for most combinations of voltage and parameters. The voltage at node 1 is designed to be about VDD/2. As the power supply voltage is raised from 4.5 volts to 5.5 volts, the (Vgs-Vt) of Q4 increases by approximately 40%. For devices Q3 and Q5 their Vgs-Vt increases by approximately 30% as VDD increases from 4.5 to 5.5 volts. To obtain the desired output voltage, the voltage at node 2 must increase only 0.100 volt while VDD is raised from 4.5 to 5.5 volts. If only device Q5 were used, the voltage at node 2 would rise too much as VDD increases. The effect of changes on the output voltage as VDD changes is shown in Fig. 5. If only device Q4 were used, node 2 would decrease as VDD increases. By choosing the correct device sizes for Q4 and Q5, the desired increase of 0.100 volt at node 2 is achieved.

To compensate for variations in device parameters, the FETs are designed in large and small widths and channel lengths. For best case parameters (highest device current) the output voltage must be higher. Therefore, the voltage at node 2 must decrease for best case (+3 sigma) parameters. The width and length of the device are a nominal value +/-the tolerance.

DW = W nominal + tolerance (equation 1)

DL = L nominal + tolerance (equation 2)

where D represents Device

W represents Width

L represents Length

For a device with a large W nominal and L nominal, the current will be insensitive to parameter variations (tolerance). The current in devices with small W nominal and L nominal will increase significantly for best case parameters (+3 sigma) versus worst case parameters (-3 sigma). Device Q3 (Fig. 4) has large geometries and devices Q4 and Q5 have small geometries so that the voltage at node 2 will decrease as parameters vary from -3 sigma to +3 sigma. For example, the following set of parameters are suitable values for devices Q3, Q4, Q5.

	Width	Length
Q3	50	6
Q4	20	3
Q5	10	3
Tolerance = ±1		

Hence, it can be seen that the width to length ratio (W/L) of device Q3 only varies 20% from nominal to $+3\sigma$ while the W/L ration of Q5 varies by 65% from nominal to $+3\sigma$.

Still referring to Fig. 4, the second compensation circuit arrangement includes devices Q7 through Q12. Each of a parallel pair of P-channel FET devices Q7 and Q10 is connected in series with an individual one of N-channel devices Q8 and Q11. Devices Q7 and Q8 are connected at node 4 which in turn is connected to the gate electrode of device Q9. The source electrode of device Q9 is connected to node 2 and the drain electrode is connected to ground potential. Similarly, devices Q10 and Q11 are connected in series at node 5 which is connected to the gate electrode of device Q12. Device Q12 is connected to node 2 and VDD. In operation, devices Q7-Q12 compensate for variations in device threshold voltage (Vt). When the P-channel threshold voltage Vt is low (Vgs - Vt large) the load device current (such as Q26), Fig. 1, will be too high. Current in device Q7 (Fig. 4) will increase and the voltage at node 4 will rise turning on device Q9. Current in device Q9 reduces the voltage at node 2 which reduces the current capability of Q6. The bias voltage rises slightly, reducing the current in the load device and in Q7. When the Vt of the P-channel devices is high (Vgs - Vt minimum) current in the load devices is too low. Current in device Q10 decreases and the voltage at node 5 drops which turns on Q12. Current in Q12 raises the voltage at node 2. A higher voltage at node 2 increases the current at Q6, reducing the bias voltage and increasing current in the load devices. Most combinations of power supply voltage and process parameters of the voltage at nodes 4 and 5 are such that devices Q8 and Q12 are off and do not have any effect on the output voltage.

The bias voltage generator can be deactivated by devices Q13-Q15 and Q17. P-channel device Q13 is connected in series with N-channel device Q14 between VDD and ground potential. When the +chip power is activated, devices Q13-Q15 cause the disabling of all dc power dissipation within the bias generator and

the Vref potential rises to the full power supply potential. Vref = Vps reduces to zero all power dissipation in the controlled elements with the design. Similarly, devices Q17 and Q15 deactivate the output of the voltage generator when a signal is applied to the Degate input allowing maximum dc power dissipation. The features associated with devices Q13-Q15, Q17 are auxiliary to the bias generator function and provide the additional function of auto-override, both for minimum and maximum power checking and testability.

Claims

1. A bias voltage generator for static circuits on a CMOS chip comprising
a first compensation circuit arrangement (14) coupled to a power supply (+VDD) and a control node, the arrangement serving to generate at the control node a control voltage signal which compensates for tolerances in the power supply and device process parameters; and
a second compensation circuit arrangement (16) coupled to the control node and serving to adjust the control voltage signal at the control node to compensate for device threshold voltage variations.

2. A bias voltage generator as claimed in claim 1, wherein the first compensation circuit arrangement includes a first circuit means (Q1, Q2) for generating a first voltage, and
a second circuit means (Q3, Q4, Q5) responsive to the first voltage to generate the control voltage at the control node.

3. A bias voltage generator as claimed in claim 2, wherein the first circuit means includes a pair of N-channel FET devices (Q1, Q2) connected in series.

4. A bias voltage generator as claimed in claim 2 or claim 3, wherein the second circuit means includes a P-channel FET device (Q3) coupled to a supply voltage source (+VDD), and a pair of N-channel FET devices (Q4, Q5) coupled in parallel relative to one another and each coupled in series relative to the P-channel device.

5. A bias voltage generator as claimed in any preceding claim, wherein the second compensation circuit arrangement includes two pairs of series-connected FET devices (Q7, Q8; Q10, Q11) positioned in a parallel configuration between a voltage supply source (+VDD) and a ground potential; and two switching FET devices (Q9, Q12) connected in series with each switching devices having its control electrode connected to an individual one of the nodes between the devices in each pair of series-connected FET devices.

6. A bias voltage generator as claimed in any preceding claim, further including an inverting circuit means (18) coupled to the control node and serving to invert the control voltage signal to the control node to produce the output voltage of the generator.

7. A bias voltage generator as claimed in any preceding claim, further including a deactivating circuit (20) coupled to the first compensation circuit arrangement for causing the latter to produce a chip-circuit deactivating control voltage at the control node.

8. A bias voltage generator as claimed in any preceding claim, further including a degating circuit means (22) coupled to the second compensation circuit arrangement for deactivating the control node.

9. An integrated circuit chip incorporating static CMOS circuits and a bias voltage generator as claimed in any preceding claim with its bias voltage output coupled to the static CMOS circuits.

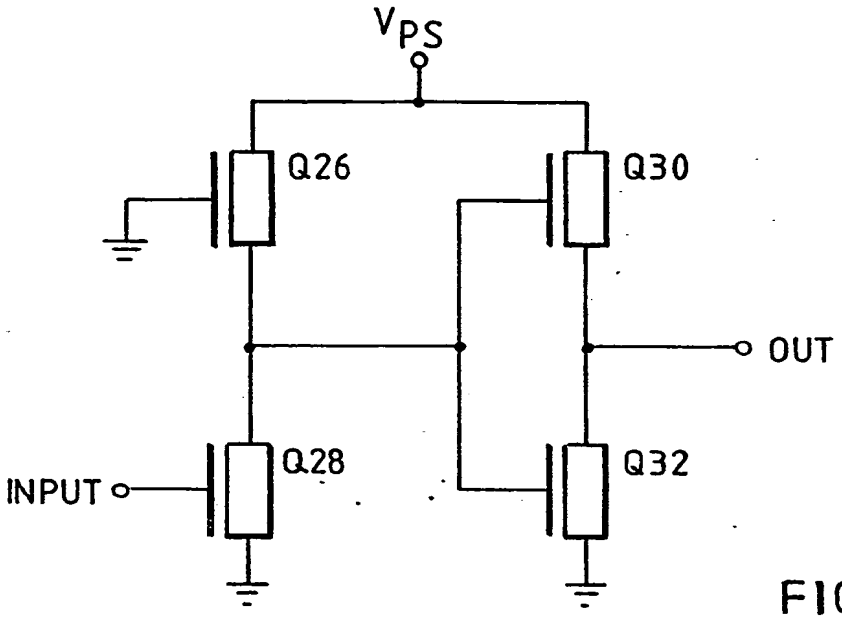

FIG. 1
PRIOR ART

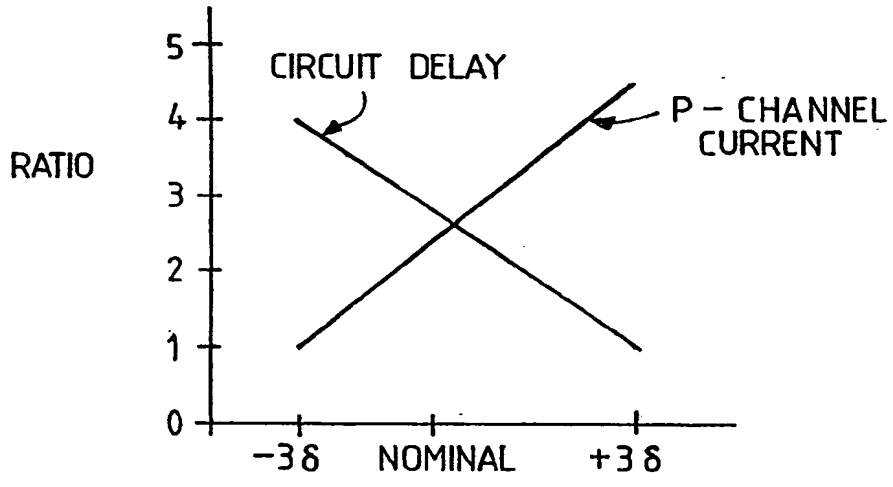

FIG. 2

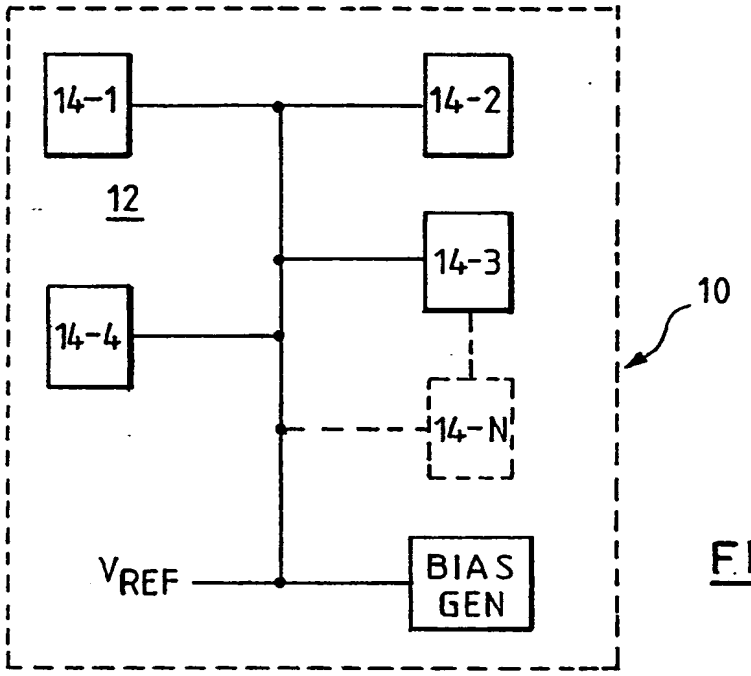
14-1
14-2
12
14-3
14-4
10
14-N
VREF
BIAS GEN

FIG. 3

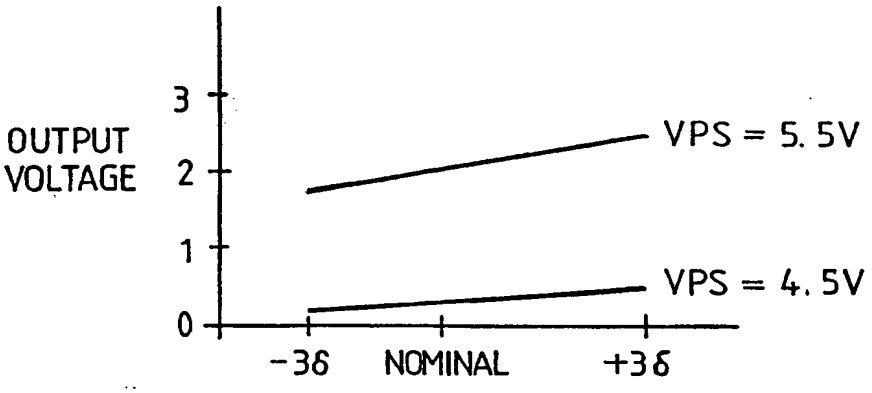
OUTPUT VOLTAGE
3
2
1
0
VPS = 5.5V
VPS = 4.5V
-3δ
NOMINAL
+3δ

FIG. 5

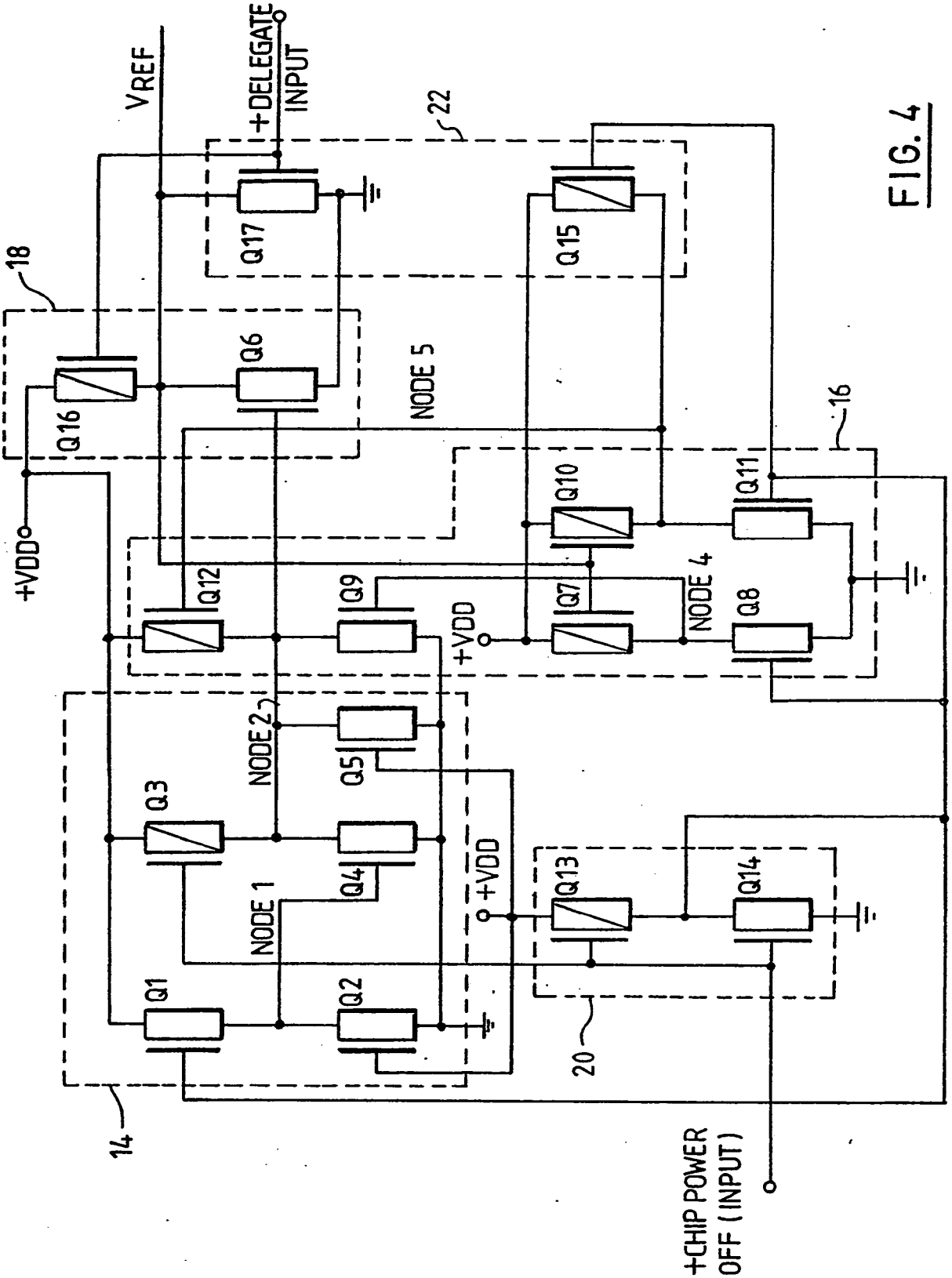
VREF
+DELEGATE INPUT
22
18
Q17
Q15
Q16
Q6
NODE 5
16
+VDD
Q10
Q11
Q12
Q9
Q7
NODE 4
Q8
+VDD
NODE 2
Q5
Q3
Q4
+VDD
Q13
Q14
NODE 1
Q1
Q2
20
14
+CHIP POWER OFF (INPUT)

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 30 7640

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	US-A-4723108 (MURPHY ET AL) * column 2, line 45 - column 3, line 54; figure 1 *	1-9	G05F3/24
A	US-A-4446383 (CONCANNON ET AL) * column 2, line 46 - column 3, line 27; figures 1-3 *	1-4	
A	US-A-4453121 (NOUFER) * column 3, line 47 - column 4, line 18; figure 2 *	1-4	
A	US-A-4645998 (SHINOHARA ET AL) * column 5, lines 1 - 25; figure 3 *	1-4	
A	US-A-4323846 (HARASZTI) * column 3, line 60 - column 5, line 25; figure 2 *	1, 5	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 NOVEMBER 1989	CLEARY F.M.

CATEGORY OF CITED DOCUMENTS

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